MASTER OF TECHNOLOGY

EMBEDDED SYSTEMS

STRUCTURE & SYLLABUS – R20

(Batches admitted from the academic year 2020 - 2021)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(Autonomous Institution-UGC, Govt. of India)

Accredited by NBA & NAAC with 'A' Grade

NIRF Indian Ranking, Accepted by MHRD, Govt. of India | Rank Band – Excellent by ARIIA, Accepted by MHRD, Govt. of India

Approved by AICTE, Affiliated to JNTUH, ISO 9001:2015 Certified Institution

Platinum Rated by AICTE-CII Survey, AAAA+ Rated by Digital Learning Magazine, AAA+ Rated by Careers 360, National Ranking-Top 100 Rank band by Outlook Magazine, 2nd Rank by CSR, National Ranking-Top 100 Rank band by Times News Magazine, 141 Rank by India Today-Best Engineering Colleges of India Rankings-2020.

Maisammaguda, Dhulapally, Secunderabad, Kompally-500100.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

Permanently Affiliated to JNTUH, Approved by AICTE, ISO 9001: 2015 Certified Institution
Accredited by NBA & NAAC with 'A' Grade
NIRF Indian Ranking 2020, Accepted by MHRD Govt. of India
AAA+ Rated by Careers 360 Magazine, Top Hundred Rank band by Outlook, 3rd Rank CSR

COURSE STRUCTURE

M. Tech (EMBEDDED SYSTEMS) COURSE STRUCTURE

M. Tech – I Semester

S.No.	SUBJECT CODE	Course Title	L	T	P	Credits
1	2055PC01	Microcontrollers & Programmable Digital Signal Processors	3	0	0	3
2	2055PC02	System Design with Embedded Linux	3	0	0	3
3		Professional Elective- I	3	0	0	3
4		Professional Elective - II	3	0	0	3
5	2055PC31	Microcontroller & Programmable Digital Signal Processors Lab	0	0	4	2
6	2055PC32	System Design with Linux Lab	0	0	4	2
7	2055PJ01	Research Methodology & IPR	2	0	0	2
8		Audit Course - I	2	0	0	0
9	2055PJ02	Technical Seminar - I	0	0	0	2
		Total	**16**	**0**	**8**	**20**

M. Tech– II Semester

S.No.	SUBJECT CODE	Course Title	L	T	P	Credits
1	2055PC03	RTL Simulation and Synthesis with PLDs	3	0	0	3
2	2055PC04	Advanced Digital Signal Processing	3	0	0	3
3		Professional Elective - III	3	0	0	3
4		Professional Elective - IV	3	0	0	3
5	2055PC33	RTL Simulation and Synthesis with PLDs Lab	0	0	4	2
6	2055PC34	Advanced Digital Signal Processing Lab	0	0	4	2
7	2055PJ03	Mini Project	0	0	4	2
8		Audit Course - 2	2	0	0	0
9	2055PJ04	Technical Seminar - 2	0	0	0	2
		Total	**14**	**0**	**12**	**20**

M. Tech– III Semester

S. No.	SUBJECT CODE	Course Title	L	T	P	Credits
1		Professional Elective - V	3	0	0	3
2		Open Elective	3	0	0	3
3	2055PJ05	Dissertation Work Review - I	0	0	12	6
4	2055PJ06	Technical Seminar - 3	0	0	0	2
		Total	**06**	**0**	**12**	**14**

M. Tech – IV Semester

S. No.	SUBJECT CODE	Course Title	L	T	P	Credits
1	2055PJ07	Dissertation Work Review - II	0	0	12	6
2	2055PJ08	Dissertation Viva-Voce	0	0	28	14
4	2055PJ09	Technical Seminar - 4	0	0	0	2
		Total	**0**	**0**	**40**	**22**

Semester	I	II	III	IV	TOTAL
Credits	20	20	14	22	**76**

PROFESSIONAL ELECTIVES			
PE-I		**PE-II**	
2055PE01	Programming Languages for Embedded Software	2055PE04	Digital System Design
2058PE02	AI & Machine Leaning	2055PE05	Parallel Processing
2055PE03	Computer Vision	2055PE06	Advanced Computer architecture
PE-III		**PE-IV**	
2055PE07	IOT and its Applications	2055PE10	Hardware and Software Co-Design
2055PE08	CMOS VLSI System Design	2055PE11	Network Security and Cryptography
2055PE09	SOC Architecture	2055PE12	Physical Design Automation
PE-V			
2055PE13	Memory Technologies		
2055PE14	Wireless Communications and Networks		
2055PE15	Wireless Sensor Networks		

AUDIT COURSES I & II	
2055AU01	1. English for Research Paper Writing
2055AU02	2. Disaster Management
2055AU03	3. Sanskrit for Technical Knowledge
2055AU04	4. Value Education
2055AU05	5. Constitution of India
2055AU06	6. Pedagogy Studies
2055AU07	7. Stress Management by yoga
2055AU08	8. Personality Development Through Life Enlightenment Skills

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PC01) MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

M.Tech I Year I Sem

L	T	P	C
3	0	0	3

Course Outcomes: At the end of this course, students will be able to

1. Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
2. Identify and characterize architecture of Programmable DSP Processors
3. Develop small applications by utilizing the ARM processor core and DSP processor based platform.

UNIT-I

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified AssemblerLanguage, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT-II

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT-III

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT-IV

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT-V

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations

TEXTBOOKS:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" , TMH , 2nd Edition

REFERENCES:

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PC02) SYSTEM DESIGN WITH EMBEDDED LINUX

M.Tech I Year I Sem L T P C
3 0 0 3

Course Outcomes: At the end of this course, students will be able to

1. Familiarity of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Understand and create Linux BSP for a hardware platform

UNIT-I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling.

Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross tool chains

UNIT-II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

UNIT-III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules

Embedded Drivers: Serial, Ethernet, I2 C, USB, Timer, Kernel Modules

UNIT-IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT-V

Building and Debugging: Bootloaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds “Mastering Embedded Linux Programming” - Second Edition, PACKT Publications Limited.
2. Karim Yaghmour, “Building Imbedded Linux Systems”, O'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design and Development”, Auerbach Publications

REFERENCES:

1. Christopher Hallinan, “Embedded Linux Primer: A Practical Real World Approach”, Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PE01) PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE (PE- I)

M.Tech I Year I Sem

L	T	P	C
3	0	0	3

Course Outcomes: At the end of this course, students will be able to

1. Write an embedded C application of moderate complexity.
2. Develop and analyze algorithms in C++.
3. Differentiate interpreted languages from compiled languages.

UNIT-I

Embedded 'C' Programming

- Bitwise operations, Dynamic memory allocation, OS services
- Linked stack and queue, Sparse matrices, Binary tree
- Interrupt handling in C, Code optimization issues
- Writing LCD drives, LED drivers, Drivers for serial port communication
- Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT-II

CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT-III

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

UNIT-IV

Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch-throw, Multiple Exceptions.

UNIT-V

Scripting Languages Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

TEXTBOOKS:

1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011

REFERENCES:

1. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999

Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE02) AI & MACHINE LEARNING (PE- I)

M.Tech I Year I Sem

L	T	P	C
3	0	0	3

Course Outcomes: At the end of this course, students will be able to

1. Understand feed forward neural networks, feedback neural networks and learning techniques.
2. Analyze fuzziness involved in various systems and fuzzy set theory.
3. Develop fuzzy logic control for applications in electrical engineering
4. Develop genetic algorithm for applications in electrical engineering.

UNIT - I

Supervised Learning (Regression/Classification)
Basic methods: Distance-based methods, Nearest-Neighbors, Decision Trees, Naive Bayes Linear models: Linear Regression, Logistic Regression, Generalized Linear Models Support Vector Machines, Nonlinearity and Kernel Methods
Beyond Binary Classification: Multi-class/Structured Outputs, Ranking

UNIT-II

Unsupervised Learning
Clustering: K-means/Kernel K-means
Dimensionality Reduction: PCA and
kernel PCA Matrix Factorization and
Matrix Completion
Generative Models (mixture models and latent factor models)

UNIT-III

Evaluating Machine Learning algorithms and Model Selection, Introduction to Statistical Learning Theory, Ensemble Methods (Boosting, Bagging, Random Forests)

UNIT-IV

Biological foundations to intelligent Systems: Artificial Neural Networks.
Single layer and Multilayer Feed Forward NN, LMS and Back Propagation.
Algorithm, Feedback networks and Radial Basis Function Networks

UNIT-V

Fuzzy Logic, Knowledge Representation and Inference Mechanism, Defuzzification Methods Fuzzy Neural Networks and some algorithms to learn the parameters of the network like GA

TEXTBOOKS:

1. Kevin Murphy, Machine Learning: A Probabilistic Perspective, MIT Press, 2012
2. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning, Springer 2009 (freely available online)
3. Christopher Bishop, Pattern Recognition and Machine Learning, Springer, 2007.
4. J M Zurada , "An Introduction to ANN",Jaico Publishing House
5. Simon Haykins, "Neural Networks", Prentice Hall

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE03) COMPUTER VISION (PE- I)

M.Tech I Year I Sem

L	T	P	C
3	0	0	3

Course Outcomes: At the end of this course, students will be able to

1. Study the image formation models and feature extraction for computer vision
2. Identify the segmentation and motion detection and estimation techniques
3. Develop small applications and detect the objects in various applications

UNIT-I

Image Formation Models Monocular imaging system • Orthographic & Perspective Projection • Camera model and Camera calibration • Binocular imaging systems, Perspective, Binocular Stereopsis: Camera and Epipolar Geometry; Homography, Rectification, DLT, RANSAC, 3-D reconstruction framework; Auto-calibration. Apparel, Binocular Stereopsis: Camera and Epipolar Geometry; Homography, Rectification, DLT, RANSAC, 3-D reconstruction framework; Auto- calibration. Apparel, Stereo vision

UNIT-II

Feature Extraction: Image representations (continuous and discrete) • Edge detection, Edge linking, corner detection, texture, binary shape analysis, boundary pattern analysis, circle and ellipse detection, Light at Surfaces; Phong Model; Reflectance Map; Albedo estimation; Photometric Stereo; Use of Surface Smoothness Constraint; Shape from Texture, color, motion and edges.

UNIT-III

Shape Representation and Segmentation: Deformable curves and surfaces • Snakes and active contours Level set representations • Fourier and wavelet descriptors • Medial representations • Multi- resolution analysis, Region Growing, Edge Based approaches to segmentation, Graph-Cut, Mean- Shift, MRFs, Texture Segmentation

UNIT-IV

Motion Detection and Estimation • Regularization theory • Optical computation • Stereo Vision Motion estimation, Background Subtraction and Modelling, Optical Flow, KLT, Spatio- Temporal Analysis, Dynamic Stereo; Motion parameter estimation • Structure from motion, Motion Tracking in Video

UNIT-V

Object recognition • Hough transforms and other simple object recognition methods • Shape correspondence and shape matching • Principal component analysis • Shape priors for recognition

REFERENCES:

1. D. Forsyth and J. Ponce, "Computer Vision - A modern approach", 2nd Edition, Pearson Prentice Hall, 2012
2. Szeliski, Richard, "Computer Vision: Algorithms and Applications", 1st Edition, Springer- Verlag London Limited, 2011.
3. Richard Hartley and Andrew Zisserman, "Multiple View Geometry in Computer Vision", 2nd Edition, Cambridge University Press, 2004.
4. K. Fukunaga, "Introduction to Statistical Pattern Recognition",2ndEdition, Morgan Kaufmann, 1990.
5. Rafael C. Gonzalez and Richard E. Woods," Digital Image Processing", 3rd Edition, Prentice Hall, 2008.
6. B. K. P. Horn, "Robot Vision", 1st Edition, McGraw-Hill, 1986.
7. E. R. Davies "Computer and Machine Vision: Theory, Algorithms, Practicalities", 4th Edition, Elsevier Inc,2012.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE04) DIGITAL SYSTEM DESIGN (PE - II)

M.Tech I Year I Sem

L T P C
3 0 0 3

Course Outcomes: At the end of this course, students will be able to

1. Design and develop real time applications using programmable devices
2. Develop skills in modeling, analyzing faults and test pattern generation
3. Design state and machine identification circuits.
4. Apply various techniques for designing circuits in electronics and communication systems.

UNIT -I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT –II

Digital Design: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT –III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT –IV

Fault Modeling& Test Pattern Generation: Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT –V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Charles H. Roth, “Fundamentals of Logic Design”, 5th Edition, Cengage Learning.
2. MironAbramovici, Melvin A. Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design”, John Wiley & Sons Inc.
3. N. N. Biswas, “Logic Design Theory”, PHI

REFERENCE BOOKS:

1. Z. Kohavi , “Switching and Finite Automata Theory”, 2nd Edition, 2001, TMH
2. Morris Mano, M.D.Ciletti, “Digital Design”, 4th Edition, PHI.
3. Samuel C. Lee , “Digital Circuits and Logic Design”, PHI

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE05) PARALLEL PROCESSING (PE - II)

M.Tech I Year I Sem

L	T	P	C
3	0	0	3

Course Outcomes: At the end of this course, students will be able to

1. Identify limitations of different architectures of computer
2. Analysis quantitatively the performance parameters for different architectures
3. Investigate issues related to compilers and instruction set based on type of architectures.

UNIT-I

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability, Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT-II

VLIW processors: Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT-III

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

UNIT-IV

Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

UNIT-V

Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

TEXTBOOKS:

1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
2. Kai Hwang, "Advanced Computer Architecture", TMH

REFERENCES:

1. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.
2. William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition
3. Kai Hwang, Zhiwei Xu, “Scalable Parallel Computing”, MGH
4. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PE06) ADVANCED COMPUTER ARCHITECTURE (PE – II)

M.Tech I Year I Sem

L	T	P	C
3	0	0	3

Course Outcomes: At the end of this course, students will be able to

1. Computational models and Computer Architectures.
2. Concepts of parallel computer models.
3. Scalable Architectures, Pipelining, Superscalar processors, multiprocessors

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.

REFERENCE BOOKS

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", Mc Graw Hill.
3. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PC31) MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB (Lab – I)

M.Tech I Year I Sem

L T P C
0 0 4 2

Course Outcomes:

At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SOC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on the LPC 2148 ARM7and DSP development boards.

List of Assignments:

Part A) Experiments to be carried out on LPC2148 ARM 7 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using timer.
2. System clock real time alteration using the PLLmodules.
3. Control intensity of an LED using PWM implemented in software andhardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. Controlling LCD Display and sending information to display.
6. Interfacing Buzzer and controlling using LPC module.
7. Interfacing LED's and Buzzer to ARM7 and accessing using switches.
8. Interfacing 7-Segment Display with ARM7 and display Hexa Decimal Numbers

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PC32) SYSTEM DESIGN WITH LINUX LAB (Lab – II)

M.Tech I Year I Sem

L T P C
0 0 4 2

List of Experiments:

1. Write a program that illustrates how to execute two commands concurrently with a command pipe.
2. Write a program in which a parent write a message to a pipe and child reads that message.
3. Write a program to create a message queue with read and write permissions to write 3 messages to it with different priority numbers.
4. Write a program to demonstrate thread synchronization with mutex locks.
5. Write client and server programs for interaction between server and client processes using Unix Domain sockets
6. Write a client and server programs for interaction between server and client processes using Internet Domain sockets.
7. Write a program that illustrates two processes communicating using shared memory.
8. Write a program that illustrates suspending and resuming processes using signals
9. Design and Develop shell Program to count number of line in a file without using WC.
10. Configuring the mail server

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PJ01) RESEARCH METHODOLOGY AND IPR

M.Tech I Year I Sem

L T P C
2 0 0 2

Prerequisite: None

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT-III:

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCES:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PC03) RTL SIMULATION AND SYNTHESIS WITH PLDs

M.Tech I Year II Sem

L T P C
3 0 0 3

Course Outcomes: At the end of the course, students will demonstrate the ability to:

1. Familiarity of Finite State Machines, RTL design using reconfigurable logic.
2. Design and develop IP cores and Prototypes with performance guarantees
3. Use EDA tools like Cadence, Mentor Graphics and Xilinx

UNIT-I

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

UNIT-II

Design entry by Verilog/VHDL/FSM, Verilog AMS.

UNIT-III

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

UNIT-IV

Design for performance, Low power VLSI design techniques. Design for testability.

UNIT-V

IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping

TEXTBOOKS:

1. Richard S. Sandige, “Modern Digital Design”, MGH, International Editions.
2. Donald D Givone, “Digital principles and Design”, TMH

REFERENCES:

1. Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning.
2. Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall.
3. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx
4. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PC04) ADVANCED DIGITAL SIGNAL PROCESSING

M.Tech I Year II Sem L T P C
3 0 0 3

Course Outcomes: At the end of this course, students will be able to

1. To understand theory of different filters and algorithms
2. To understand theory of multirate DSP, solve numerical problems and write algorithms
3. To understand theory of prediction and solution of normal equations
4. To know applications of DSP at block level.

UNIT-I
Overview of DSP, Characterization in time and frequency, FFT Algorithms, Digital filter design and structures: Basic FIR/IIR filter design &structures, design techniques of linear phase FIR filters,IIR filters by impulse invariance, bilinear transformation, FIR/IIR Cascaded lattice structures, parallel realization of IIR.

UNIT-II
Multi rate DSP, Decimators and Interpolators, Sampling rate conversion, multistage decimator & interpolator, poly phase filters, QMF, digital filter banks, Applications in subband coding.

UNIT-III
Linear prediction & optimum linear filters, stationary random process, forward-backward linear prediction filters, solution of normal equations, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction.

UNIT-IV
Adaptive Filters, Applications, Gradient Adaptive Lattice, Minimum mean square criterion, LMS algorithm, Recursive Least Square algorithm

UNIT-V
Estimation of Spectra from Finite-Duration Observations of Signals. Nonparametric Methods for Power Spectrum Estimation, Parametric Methods for Power Spectrum Estimation, Minimum- Variance Spectral Estimation, Eigen analysis Algorithms for Spectrum Estimation.

TEXTBOOKS:

1. J. G. Proakis and D.G. Manolakis, "Digital signal processing: Principles, Algorithm and Applications", 4th Edition, Prentice Hall, 2007.
2. N. J. Fliege, "Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets", 1st Edition, John Wiley and Sons Ltd, 1999.

REFERENCES:

1. Bruce W. Suter, "Multirate and Wavelet Signal Processing",1st Edition, Academic Press, 1997.
2. M. H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley & Sons Inc., 2002.
3. S. Haykin, "Adaptive Filter Theory", 4th Edition, Prentice Hall, 2001.
4. D. G. Manolakis, V. K. Ingle and S. M. Kogon, "Statistical and Adaptive Signal Processing", McGraw Hill, 2000

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE07) IOT AND ITS APPLICATIONS (PE – III)

M.Tech I Year II Sem L T P C
3 0 0 3

Course Outcomes: At the end of this course, students will be able to

1. Understand the concept of IOT and M2M
2. Study IOT architecture and applications in various fields
3. Study the security and privacy issues in IOT.

UNIT-I

IoT& Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics.

UNIT-II

M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value
chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

UNIT-III

IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

UNIT-IV

IoT Applications for Value Creations Introduction, IoT applications for industry: Future Factory Concepts, Brownfield IoT, Smart Objects, Smart Applications, Four Aspects in

your Business to Master IoT, Value Creation from Big Data and Serialization, IoT for Retailing Industry, IoT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, eHealth.

UNIT-V

Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues,

TEXTBOOKS

1. Vijay Madisetti and Arshdeep Bahga, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014.
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1st Edition, Apress Publications, 2013.
3. Cuno Pfister, "Getting Started with the Internet of Things", O Reilly Media, 2011.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE08) CMOS VLSI SYSTEM DESIGN (PE-III)

M.Tech I Year II Sem

L T P C
3 0 0 3

Course Outcomes: At the end of this course, students will be able to

1. Describe the Microelectronics and MOS Technologies
2. Sketch the Layout Design.
3. Discuss the Floor Planning, Architecture Design.
4. Demonstrate a clear understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
5. Use the physical design aspects to draw the basic gates using the stick and layout diagrams.

UNIT-I

MOS Transistor: Introduction, Ideal I-V Characteristics, C-V Characteristics, Non ideal I-V Effects, DC Transfer Characteristics.

CMOS Process Technology: CMOS Technologies, Layout Design Rules, CMOS Process Enhancements, Technology related CAD Issues.

UNIT-II

Circuit Characterization: Delay Estimation, Logical effort and Transistor Sizing, Power Dissipation, Interconnect, Design Margin, Reliability, Scaling.

UNIT-III

Combinational and Sequential Circuit Design: Circuit Families, More circuit families, Low power Logic Design, Comparison of Circuit Families, Sequencing Static Circuits, Circuit Design of Latches and Flip-Flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers.

UNIT-IV

Datapath Subsystems: Addition, Subtraction, Comparators, Counters, Boolean Logical Operations, Coding, Shifters, Multiplication, Division.

Array Subsystems: SRAM, DRAM, Read-only Memory, Serial Access Memories, Content addressable Memory, PLAs, Array Yield, Reliability and Self-Test.

UNIT-V

Design Methodology and Tools: Design Methodology, Design Flows, Design Economics, Data Sheets and Documentation, CMOS Physical Design Styles, Interchange Formats. **Special Purpose Subsystem:** Packaging.

TEXTBOOKS:

1. Neil Weste, David Harris, Ayan Banerjee, “CMOS VLSI DESIGN”, 3rd Edition, Pearson.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE09) SOC ARCHITECTURE (PE-III)

M.Tech I Year II Sem

L T P C
3 0 0 3

Course Outcomes: At the end of this course, students will be able to

1. Introduction to SOC Architecture and design.
2. Processor design Architectures and limitations
3. To acquires the knowledge of memory architectures on SOC.
4. To understands the interconnection strategies and their customization on SOC.

UNIT – I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Michael J. Flynn and Wayne Luk, "Computer System Design System-on-Chip", Wiley India Pvt. Ltd.
2. Steve Furber, "ARM System on Chip Architecture ", 2nd Edition, 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Ricardo Reis, ""Design of System on a Chip: Devices and Components", 1st Edition, 2004, Springer
2. Jason Andrews, "Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)", Newnes, BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques", 2001, Kluwer Academic Publishers.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PE10)) HARDWARE AND SOFTWARE CO-DESIGN (PE-IV)

M.Tech I Year II Sem L T P C
3 0 0 3

Course Outcomes

1. To acquire the knowledge on various models of Co-design.
2. To explore the interrelationship between Hardware and software in a embedded system
3. To acquire the knowledge of firmware development process and tools during Co-design.
4. Understand validation methods and adaptability.

UNIT I

Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent
computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

REFERENCES:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami,Kluwer Academic Publishers, 2002.
3. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PE11) NETWORK SECURITY AND CRYPTOGRAPHY (PE-IV)

M.Tech I Year II Sem L T P C
3 0 0 3

Course Outcomes: At the end of the course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

UNIT-I:

Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT-II

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT-III

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT-IV

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT-V

Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations,

Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

TEXT BOOKS:

1. William Stallings, “Cryptography and Network Security, Principles and Practices”, Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security, Private Communication in a Public World”, Prentice Hall, 2nd Edition

REFERENCES:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, “Security Architecture, Design Deployment and Operations”, RSA Pres,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, “Inside Network Perimeter Security”, Pearson Education, 2nd Edition
3. Richard Bejtlich, “The Practice of Network Security Monitoring: Understanding Incident Detection and Response”, William Pollock Publisher, 2013.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE12) PHYSICAL DESIGN AUTOMATION (PE-IV)

M.Tech I Year II Sem

L T P C
3 0 0 3

Course Outcomes: At the end of the course, students will be able to:

1. Study automation process for VLSI System design.
2. Understanding of fundamentals for various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

UNIT- I

Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT- II

Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT- III

Placement: Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT- IV

Global routing: Problem formulation, classification of global routing, Maze routing algorithms, Line- Probe algorithms, and shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.

Detailed Routing: Problem formulation, classification, Single layer, two layer, three layer and Multi- Layer channel routing, Algorithms, Switch box routing.

UNIT- V

Over the Cell Routing - Single layer and two-layer routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing.

Via Minimization: Constraint and Unconstrained via minimization.

Clock and Power Routing: Clocking schemes, design considerations for the clock ,Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS

1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005,
2. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PC33) RTL SIMULATION AND SYNTHESIS WITH PLDS LAB (Lab – III)

M.Tech I Year II Sem

L T P C
0 0 4 2

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
2. Use EDA tools like Cadence, Mentor Graphics and Xilinx or equivalent tools

List of Experiments:

1. Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3. Vending machines - Traffic Light controller, ATM, elevator control.
4. PCI Bus & arbiter and downloading on FPGA.
5. UART/ USART implementation in Verilog.
6. Realization of single port SRAM in Verilog.
7. Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
8. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PC34) ADVANCED DIGITAL SIGNAL PROCESSING LAB (Lab – IV)

M.Tech I Year II Sem

L T P C
0 0 4 2

Note: Minimum of 10 Experiments have to be conducted

List of Experiments:

1. Basic Operations on Signals, Generation of Various Signals and finding its FFT.
2. Program to verify Decimation and Interpolation of a given Sequences.
3. Program to Convert CD data into DVD data
4. Generation of Dual Tone Multiple Frequency (DTMF) Signals
5. Plot the Periodogram of a Noisy Signal and estimate PSD using Periodogram and Modified Periodogram methods
6. Estimation of Power Spectrum using Bartlett and Welch methods
7. Verification of Autocorrelation Theorem
8. Parametric methods (Yule-Walker and Burg) of Power Spectrum Estimation
9. Estimation of data series using Nth order Forward Predictor and comparing to the Original Signal
10. Design of LPC filter using Levinson-Durbin Algorithm
11. Computation of Reflection Coefficients using Schur Algorithm
12. To study Finite Length Effects
13. ECG signal compression
14. Design and Simulation of Notch Filter to remove 60 Hz Hum/any unwanted frequency component of given Signal (Speech/ECG)

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055PE13) MEMORY TECHNOLOGIES (PE – V)

M.Tech II Year (III Sem) L T P C
3 0 0 3

Course Outcomes: At the end of the course, students will be able to:

1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
3. Know, how of the state-of-the-art memory chip design

UNIT- I

Random Access Memory Technologies: Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT-II

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

UNIT-III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT-IV

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

UNIT-V

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

TEXTBOOKS:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition

REFERENCES:

1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability , PHI

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE14) WIRELESS COMMUNICATIONS AND NETWORKS (PE – V)

M.Tech II Year (III Sem) L T P C
3 0 0 3

Course Outcomes: At the end of this course, students will be able to

1. Understand the principles of wireless communications.
2. Understand fundamentals of wireless networking
3. Understand cellular system design concepts.
4. Analyze various multiple access schemes used in wireless communication.
5. Understand wireless wide area networks and their performance analysis.

UNIT – I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT – II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models-LongleyRyce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT – III

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models

for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT – IV

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Nonlinear Equalization Decision Feedback Equalization (DFE), Maximum Likelihood Sequence Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean

Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT – V

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, HiperLan, WLL.

TEXT BOOKS:

1. Theodore, S. Rappaport, “Wireless Communications, Principles, Practice”, 2nd Ed., 2002, PHI.
2. Andrea Goldsmith, “Wireless Communications”, 2005 Cambridge University Press.
3. KavehPahLaven and P. Krishna Murthy, “Principles of Wireless Networks”, 2002, PE
4. GottapuSasibhushana Rao, “Mobile Cellular Communication”, Pearson Education, 2012.

REFERENCE BOOKS:

1. KamiloFeher, “Wireless Digital Communications”, 1999, PHI.
2. William Stallings, “Wireless Communication and Networking”, 2003, PHI.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055PE15) WIRELESS SENSOR NETWORKS (PE – V)

M.Tech II Year (III Sem) L T P C
3 0 0 3

Course Objectives

1. To acquire the knowledge about various architectures and applications of Sensor Networks
2. To understand issues, challenges and emerging technologies for wireless sensor networks
3. To learn about various routing protocols and MAC Protocols
4. To understand various data gathering and data dissemination methods
5. To Study about design principals, node architectures, hardware and software required for implementation of wireless sensor networks.

Course Outcomes: Upon completion of the course, the student will be able to:

1. Analyze and compare various architectures of Wireless Sensor Networks
2. Understand Design issues and challenges in wireless sensor networks
3. Analyze and compare various data gathering and data dissemination methods.
4. Design, Simulate and Compare the performance of various routing and MAC protocol

UNIT -I:

Introduction to Sensor Networks, unique constraints and challenges, Advantage of Sensor Networks, Applications of Sensor Networks, Types of wireless sensor networks

UNIT –II

Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for Wireless Sensor Networks. Issues and challenges in wireless sensor networks

UNIT –III

Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol, IEEE 802.15.4 standard and ZigBee

UNIT -IV

Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion; Quality of a sensor network; Real-time traffic support and security protocols.

UNIT -V

Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication. Single-node architecture, Hardware components & design constraints, Operating systems and execution environments, introduction to TinyOS and nesC.

TEXT BOOKS:

1. Ad-Hoc Wireless Sensor Networks- C. Siva Ram Murthy,B. S. Manoj, Pearson
2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

REFERENCE BOOKS:

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking – William Stallings, 2003, PHI.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055AU01) ENGLISH FOR RESEARCH PAPER WRITING (Audit Course I & II)

M.Tech I Year

L T P C
2 0 0 0

Prerequisite: None

Course objectives: Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first- time submission

UNIT-I:

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT-II:

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

UNIT-III:

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV:

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V:

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, and skills are needed when writing the Conclusions. Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

TEXT BOOKS/ REFERENCES:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055AU02) DISASTER MANAGEMENT (Audit Course I & II)

M.Tech I Year L T P C
2 0 0 0

Prerequisite: None

Course Objectives: Students will be able to

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- critically understand the strengths and weaknesses of disaster management approaches,
- planning and programming in different countries, particularly their home country or the countries they work in

UNIT-I:

Introduction:
Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics

UNIT-II:

Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT-III:

Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT-IV:

Risk Assessment Disaster Risk:

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT-V:

Disaster Mitigation:

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

TEXT BOOKS/ REFERENCES:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, Pardeep Et. Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Goel S. L., Disaster Administration and Management Text and Case Studies", Deep &Deep Publication Pvt. Ltd., New Delhi.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055AU03) SANSKRIT FOR TEACHINICAL KNOWLEDGE (Audit Course I & II)

M.Tech I Year

L T P C
2 0 0 0

Prerequisite: None

Course Objectives:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Course Outcomes: Students will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science & technology can be understood
- Being a logical language will help to develop logic in students

UNIT-I:
Alphabets in Sanskrit,

UNIT-II:
Past/Present/Future Tense, Simple Sentences

UNIT-III:
Order, Introduction of roots,

UNIT-IV:
Technical information about Sanskrit Literature

UNIT-V:
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

TEXT BOOKS/ REFERENCES:

1. "Abhyaspustakam" – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(UGC AUTONOMOUS)

(2055AU04) VALUE EDUCATION (Audit Course I & II)

M.Tech I Year

L T P C
2 0 0 0

Prerequisite: None

Course Objectives: Students will be able to

- Understand value of education and self- development
- Imbibe good values in students
- Let the should know about the importance of character

Course outcomes: Students will be able to

- Knowledge of self-development
- Learn the importance of Human values
- Developing the overall personality

UNIT-I:

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT-II:

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT-III:

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness.

UNIT-IV:

Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT-V:

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation, Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

TEXT BOOKS/ REFERENCES:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055AU05) CONSTITUTION OF INDIA (Audit Course I & II)

M.Tech I Year L T P C
2 0 0 0

Prerequisite: None

Course Objectives: Students will be able to:
- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes: Students will be able to:
- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

UNIT-I:
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working),
Philosophy of the Indian Constitution: Preamble**,** Salient Features.

UNIT-II:
Contours of Constitutional Rights & Duties: Fundamental Rights Right to Equality**,** Right to Freedom**,** Right against Exploitation**,** Right to Freedom of Religion**,** Cultural and Educational Rights**,** Right to Constitutional Remedies, Directive Principles of State Policy**,** Fundamental Duties.

UNIT-III:
Organs of Governance: Parliament**,** Composition**,** Qualifications and Disqualifications**,** Powers and Functions**,** Executive**,** President**,** Governor**,** Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualification, Powers and Functions.

UNIT-IV:

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT-V:

Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

TEXT BOOKS/ REFERENCES:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055AU06) STUDIES (Audit Course I & II)

M.Tech I Year

L T P C
2 0 0 0

Prerequisite: None

Course Objectives: Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes: Students will be able to understand:

- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT-I:

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT-II:

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT-III:

Evidence on the effectiveness of pedagogical practices, Methodology for the indepth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the scho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT-IV:

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT-V:

Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOKS/ REFERENCES:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055AU07) STRESS MANAGEMENT BY YOGA (Audit Course I & II)

M.Tech I Year

L T P C
2 0 0 0

Prerequisite: None

Course Objectives:
- To achieve overall health of body and mind
- To overcome stress

Course Outcomes: Students will be able to:
- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

UNIT-I:
Definitions of Eight parts of yog. (Ashtanga)

UNIT-II:
Yam and Niyam.

UNIT-III:
Do`s and Don't's in life.
i) Ahinsa, satya, astheya, bramhacharya and aparigraha
ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT-IV:
Asan and Pranayam

UNIT-V:
i) Various yog poses and their benefits for mind & body
ii) Regularization of breathing techniques and its effects-Types of pranayam

TEXT BOOKS/ REFERENCES:

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN
(UGC AUTONOMOUS)

(2055AU08) PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT (Audit Course I & II)

M.Tech I Year

L T P C
2 0 0 0

Prerequisite: None

Course Objectives:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes: Students will be able to

- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT-I:

Neetisatakam-Holistic development of personality

1. Verses- 19,20,21,22 (wisdom)
2. Verses- 29,31,32 (pride & heroism)
3. Verses- 26,28,63,65 (virtue)

UNIT-II:

Neetisatakam-Holistic development of personality

1. Verses- 52,53,59 (dont's)
2. Verses- 71,73,75,78 (do's)

UNIT-III:

Approach to day to day work and duties.

1. Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
2. Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
3. Chapter 18-Verses 45, 46, 48.

UNIT-IV:

Statements of basic knowledge.

1. Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
2. Chapter 12 -Verses 13, 14, 15, 16,17, 18
3. Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V:

1. Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
2. Chapter 4-Verses 18, 38,39

3. Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.