MASTER OF TECHNOLOGY

EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABUS

(Batches admitted from the Academic Year 2018 - 2019)

MALLA REDDY ENGINEERING COLLEGE FOR WOMEN

(Autonomous Institution-UGC, Govt. of India)

Accredited by NBA & NAAC with 'A' Grade, UGC, Govt. of India

NIRF Indian Ranking–2018, Accepted by MHRD, Govt. of India

Permanently Affiliated to JNTUH, Approved by AICTE, ISO 9001:2015 Certified Institution

AAAA+ Rated by Digital Learning Magazine, AAA+ Rated by Careers 360 Magazine

6th Rank CSR, Platinum Rated by AICTE-CII Survey, Top 100 Rank band by ARIIA, MHRD, Govt. of India

National Ranking-Top 100 Rank band by Outlook, National Ranking-Top 100 Rank band by Times News Magazine

Maisammaguda, Dhullapally, Secunderabad, Kompally-500100

M. Tech (EMBEDDED SYSTEMS) COURSE STRUCTURE

M. Tech – I Semester (I Semester)

S.NO	SUBJECT CODE	SUBJECT	L	T	P	C	MAX MARKS	
							INT. MARKS	EXT. MARKS
1	1855PC01	Embedded System Design	4	0	0	4	30	70
2	1855PC02	ARM Processor Architectures	4	0	0	4	30	70
3	1855PC03	Real Time Operating Systems	4	0	0	4	30	70
4		Professional Elective-1	3	0	0	3	30	70
5		Professional Elective-2	3	0	0	3	30	70
6		Open Elective-1	3	0	0	3	30	70
7	1855PC31	Embedded Systems Laboratory	0	0	3	2	30	70
8	1855PR01	Technical seminar- I	0	0	0	2	100	-
		TOTAL	**21**	**0**	**3**	**25**	**310**	**490**

M. Tech– II Semester

S.NO	SUBJECT CODE	SUBJECT	L	T	P	C	MAX MARKS	
							INT. MARKS	EXT. MARKS
1	1855PC04	Embedded Computing	4	0	0	4	30	70
2	1855PC05	System on Chip Architecture	4	0	0	4	30	70
3	1855PC06	Sensors and Actuators	4	0	0	4	30	70
4		Professional Elective -3	**3**	**0**	**0**	**3**	30	70
5		Professional Elective -4	**3**	**0**	**0**	**3**	30	70
6		Open Elective-2	**3**	**0**	**0**	**3**	30	70
7	1855PC32	Advanced Embedded Systems Laboratory	0	0	3	2	30	70
8	1855PR02	Technical Seminar - II	0	0	0	2	100	-
		TOTAL	**21**	**0**	**3**	**25**	**310**	**490**

M. Tech –III Semester

S.NO	SUBJECT CODE	SUBJECT	L	T	P	C	MAX MARKS	
							INT. MARKS	EXT. MARKS
1	1855PR03	Technical Seminar - III	0	0	0	2	100	-
2	1855 PR04	Comprehensive Viva-Voce	0	0	0	4	-	100
3	1855 PR05	Project work Review I	0	0	11	4	50	-
4	1855 PR06	Project work Review II	0	0	11	4	50	-
		TOTAL	**0**	**0**	**22**	**14**	**200**	**100**

M. Tech – IV Semester

S.NO	SUBJECT CODE	SUBJECT	L	T	P	C	MAX MARKS	
							INT. MARKS	EXT. MARKS
1	1855 PR07	Technical Seminar -IV	0	0	0	2	100	-
2	1855 PR08	Project work Review III	0	0	24	8	100	-
3	1855 PR09	Project Evaluation (Viva-Voce)	0	0	0	16	-	100
		TOTAL	**0**	**0**	**24**	**26**	**200**	**100**

SEMISTER	I sem	II sem	III sem	IV sem	TOTAL
CREDITS	25	25	14	26	90

PROFESSIONAL ELECTIVES					
PE-I		**PE-II**		**PE-III**	
1855PE01	Advanced Computer Architecture	**1855PE04**	Digital System Design	**1855PE07**	Design for Testability
1855PE02	CMOS VLSI Design	**1855PE05**	Embedded C	**1805PE08**	Wireless Communications and Networks
1855PE03	CPLD and FPGA Architectures and Applications	**1855PE06**	TCP / IP Internetworking	**1812PE09**	Scripting Languages
PE-IV					
1855PE10	Advanced Digital Signal Processing				
1855PE11	Network Security and Cryptography				
1855PE12	Hardware Software Co-Design				

List of Open Electives offered by Various Departments for M.Tech.

S.No	Name of the Department Offering Open Electives	Open Elective –I (Semester- I)	Open Elective –II (Semester –II)
1	**Electronics & Communication Engineering**	**1855OE01:** Principles of Electronic Communications	**1855OE02:** Industrial Instrumentation **1855OE03:** Principles of Wireless Communications and Networks
2	**Computer Science & Engineering**	**1858OE01:** Cyber Security	**1858OE02:** Machine Learning **1805OE03:** Big Data With R

SYLLABUS

I YEAR M.Tech - I SEM

(I SEMESTER)

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(1855PC01) EMBEDDED SYSTEM DESIGN (PC-1)

L T P C
4 0 0 4

UNIT -I

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Shibu K.V, "Introduction to Embedded Systems", McGraw Hill.

REFERENCE BOOKS:

1. Raj Kamal, "Embedded Systems", TMH.
2. Frank Vahid, Tony Givargis, "Embedded System Design", John Wiley.
3. Lyla, "Embedded Systems", Pearson, 2013
4. David E. Simon, "An Embedded Software Primer", Pearson Education.

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(1855PC02) ARM PROCESSOR ARCHITECTURES (PC-2)

L T P C
4 0 0 4

UNIT – I

ARM Architecture and Instruction Set: ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT – II

ARM Programming Model: Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Interrupts, Software Interrupt Instructions, Exception handling

UNIT – III

ARM Programming using High Level Language: Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT – IV

Memory Management: Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

UNIT – V

Integer and Floating Point Arithmetic on ARM: Double precision Integer Multiplication, Division, Square roots, Endian Reversal and Bit Operations, Random Number Generation, DSP on ARM – FIR filters, IIR filters.

TEXT BOOKS:

1. Andrew N. Sloss, Dominic Symes, Chris Wright, "ARM Systems Developer's Guides-Designing & Optimizing System Software", 2008, Elsevier.

REFERENCE BOOKS:

1. Jonathan W. Valvano – Brookes / Cole, "Embedded Microcomputer Systems, Real Time Interfacing", 1999, Thomas Learning.

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(1855PC03) REAL TIME OPERATING SYSTEMS (PC-3)

L T P C
4 0 0 4

UNIT – I

Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT – II

Real Time Operating Systems: Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use

UNIT – III

Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT – IV

Exceptions, Interrupts and Timers: Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT – V

Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

TEXT BOOKS:

1. Qing Li, "Real Time Concepts for Embedded Systems", Elsevier, 2011

REFERENCE BOOKS:

1. Rajkamal, "Embedded Systems- Architecture, Programming, and Design", 2007, TMH.
2. W. Richard Stevens, Stephan A. Rago, "Advanced UNIX Programming", 2006, 2nd Edition, Pearson.
3. Dr. Craig Hollabaugh, "Embedded Linux: Hardware, Software and Interfacing", 2008, 1st Edition, Pearson.

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(1855PE01) **ADVANCED COMPUTER ARCHITECTURE (PE-1)**

L	T	P	C
3	0	0	3

UNIT- I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and

their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II

Pipelines: Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT – III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, An Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design : Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGrawHill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture, and Parallel Processing", McGraw Hill.,
3. DezsoSima, Terence Fountain, Peter Kacsuk , "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

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(1855PE02 **CMOS VLSI DESIGN (PE-1)**

L	T	P	C
3	0	0	3

UNIT-I

MOS Transistor: Introduction, Ideal I-V Characteristics, C-V Characteristics, Non ideal I-V Effects, DC Transfer Characteristics.

CMOS Process Technology: CMOS Technologies, Layout Design Rules, CMOS Process Enhancements, Technology related CAD Issues.

UNIT-II

Circuit Characterization: Delay Estimation, Logical effort and Transistor Sizing, Power Dissipation, Interconnect, Design Margin, Reliability, Scaling.

UNIT-III

Combinational and Sequential Circuit Design: Circuit Families, More circuit families, Low power Logic Design, Comparison of Circuit Families, Sequencing Static Circuits, Circuit Design of Latches and Flip-Flops, Static Sequencing Element Methodology, Sequencing Dynamic Circuits, Synchronizers.

UNIT-IV

Datapath Subsystems: Addition, Subtraction, Comparators, Counters, Boolean Logical Operations, Coding, Shifters, Multiplication, Division.

Array Subsystems: SRAM, DRAM, Read-only Memory, Serial Access Memories, Content addressable Memory, PLAs, Array Yield, Reliability and Self-Test.

UNIT-V

Design Methodology and Tools: Design Methodology, Design Flows, Design Economics, Data Sheets and Documentation, CMOS Physical Design Styles, Interchange Formats. **Special Purpose Subsystem:** Packaging.

TEXTBOOKS:

1. Neil Weste, David Harris, Ayan Banerjee, "CMOS VLSI DESIGN", 3rd Edition, Pearson.

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(1855PE03) **CPLD AND FPGA ARCHITECTURES AND APPLICATIONS (PE-1)**

L T P C
3 0 0 3

UNIT-I

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –IV

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, TheActel ACT1, ACT2 and ACT3 Architectures.

UNIT –V

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer International Edition.
2. Charles H. Roth Jr, LizyKurian John, "Digital Systems Design", Cengage Learning.

REFERENCE BOOKS:

1. John V. Oldfield, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley India.
2. Pak K. Chan/SamihaMourad, "Digital Design Using Field Programmable Gate Arrays", Pearson Low Price Edition.
3. Ian Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier, Newnes.

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(1855PE04) **DIGITAL SYSTEM DESIGN (PE-2)**

L	T	P	C
3	0	0	3

UNIT -I

Minimization and Transformation of Sequential Machines: The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT –II

Digital Design: Digital Design Using ROMs, PALs and PLAs, BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT –III

SM Charts: State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT –IV

Fault Modeling& Test Pattern Generation: Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model. Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT –V

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Charles H. Roth, "Fundamentals of Logic Design", 5th Edition, Cengage Learning.
2. MironAbramovici, Melvin A. Breuer and Arthur D. Friedman, "Digital Systems Testing and Testable Design", John Wiley & Sons Inc.
3. N. N. Biswas, "Logic Design Theory", PHI

REFERENCE BOOKS:

1. Z. Kohavi , "Switching and Finite Automata Theory", 2nd Edition, 2001, TMH
2. Morris Mano, M.D.Ciletti, "Digital Design", 4th Edition, PHI.
3. Samuel C. Lee , "Digital Circuits and Logic Design", PHI

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(1855PE05) **EMBEDDED C (PE-2)**

L	T	P	C
3	0	0	3

UNIT – I

Programming Embedded Systems in C: Introduction ,What is an embedded system, Which processor should you use, Which programming language should you use, Which operating system should you use, How do you develop embedded software, Conclusions.

Introducing the 8051 Microcontroller Family: Introduction, What's in a name, The external interface of the Standard 8051, Reset requirements ,Clock frequency and performance, Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption ,Conclusions.

UNIT – II

Reading Switches: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version), Example: Reading and writing bits (generic version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code), Example: Counting goats, Conclusions.

UNIT – III

Adding Structure to the Code: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example, Example: Restructuring the goat-counting example, Further examples, Conclusions.

UNIT – IV

Meeting Real-Time Constraints: Introduction, Creating 'hardware delays' using Timer 0 and Timer 1, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, Why not use Timer 2?, The need for 'timeout' mechanisms, Creating loop timeouts, Example: Testing loop timeouts, Example: A more reliable switch interface, Creating hardware timeouts, Example: Testing a hardware timeout, Conclusions.

UNIT – V

Case Study: Intruder Alarm System: Introduction, The software architecture, Key software components used in this example, running the program, the software, Conclusions.

TEXT BOOKS:

1. Michael J. Pont, "Embedded C", 2nd Edition, Pearson Education, 2008

REFERENCE BOOKS:

Nigel Gardner, "PIC micro MCU C-An introduction to programming", The Microchip PIC in CCS C.

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(1855PE06) **CP / IP INTERNETWORKING (PE-2)**

L	T	P	C
3	0	0	3

UNIT - I

Network Models: Layered Tasks, The OSI Model, Layers in OSI Model, TCP/IP Protocol suite, Addressing.

Connecting devices: Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks.

UNIT – II

Internetworking Concepts: Principles of Internetworking, Connectionless Interconnection, Application Level Interconnection, Network Level Interconnection, Properties of the Internet, Internet Architecture, Interconnection through IP Routers

TCP, UDP & IP: TCP Services, TCP Features, Segment, A TCP Connection, Flow Control, Error Control, Congestion Control, Process to Process Communication, User Datagram, Checksum, UDP Operation, IP Datagram, Fragmentation, Options, IP Addressing: Classful Addressing, IPV6.

UNIT - III

Congestion and Quality of Service: Data Traffic, Congestion, Congestion Control, Congestion Control in TCP, Congestion Control in Frame Relay, Source Based Congestion Avoidance, DEC Bit Scheme, Quality of Service, Techniques to Improve QOS: Scheduling, Traffic Shaping, Admission Control, Resource Reservation, Integrated Services and Differentiated Services.

UNIT - IV

Queue Management: Concepts of Buffer Management, Drop Tail, Drop Front, Random Drop, Passive Buffer Management Schemes, Drawbacks of PQM, Active Queue Management: Early Random Drop, RED Algorithm.

UNIT - V

Stream Control Transmission Protocol: SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

Mobile Network Layer: Entities and Terminology, IP Packet Delivery, Agents, Addressing, Agent Discovery, Registration, Tunneling and Encapsulating, Inefficiency in Mobile IP.

Mobile Transport Layer : Classical TCP Improvements, Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast Recovery, Transmission, Timeout Freezing, Selective Retransmission, Transaction Oriented TCP.

TEXT BOOKS:

1. Behrouz A Forouzan, "TCP/IP Protocol Suite", 3rd Edition, TMH.
2. B.A. Forouzan, "Data communication & Networking", 4th Edition, TMH.

REFERENCES:

1. MahbubHasan& Raj Jain, " High performance TCP/IP Networking", PHI -2005
2. Douglas. E.Comer, "Internetworking with TCP/IP ", Volume I PHI
3. Larry L. Perterson and Bruce S. Davie , "Computer Networks- A Systems Approach", 2011, Morgan Kaufmann
4. JochenSchiiler, "Mobile Communications" , Pearson , 2nd Edition.

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(1855PC31) **EMBEDDED SYSTEMS LABORATORY**

L	T	P	C
0	0	3	2

Note: Minimum of 10 Experiments have to be conducted

Part-I

A. Write a program
   i. Write a simple program to print "hello world"
   ii. Write a simple program to show a delay.
   iii. Write a program for counting the number of times that a switch is pressed & released.
   iv. Write a c program to test loop time outs.
   v. Write a c program to test hardware based timeout loops.
   vi. Illustrate the use of port header file (port M) using an interface consisting of a keypad and liquid crystal display.

B. Write a program to create a portable hardware delay.

C. Write a loop application to copy values from P1 to P2

D. Develop a simple EOS showing traffic light sequencing.

E. Write a program to drive SEOS using Timer 0.

Part-II

The following programs are to be implemented on ARM Processor

1. Simple assembly program for addition, Subtraction, Multiplication, Division, Operating Modes, System Calls and Interrupts, Loops, Branches.
2. Write an Assembly program to configure and control general purpose input/output (GPIO) port pins
3. To read digital values from external peripherals and execute them with the target board
4. Program for reading and writing of a file
5. To demonstrate time delay program using built in timer / counter feature on IDE environment
6. To demonstrate a simple interrupt handler and setting up a timer
7. Program to demonstrate a simple interrupt handlers. Press button to generate an interrupt and trace the program flow with debug terminal
8. Program to interface 8 Bit LED and Switch Interface
9. Program to implement Buzzer Interface on IDE environment

M.Tech - I YEAR

(EMBEDDED SYSTEMS)

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(1855PC04) EMBEDDED COMPUTING (PC - 4)

L	T	P	C
4	0	0	4

UNIT – I

Programming on Linux Platform:

System Calls, Scheduling, Memory Allocation, Timers, Embedded Linux, Root File System, Busy Box. **Operating System Overview**: Processes, Tasks, Threads, Multi-Threading, Semaphore, Message Queue.

UNIT – II

Introduction to Software Development Tools:

GNU GCC, make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches, lint, code profiling tools,.

UNIT – III

Interfacing Modules:

Sensor and actuator interface, data transfer and control, GPS, GSM module interfacing with data processing and display, OpenCV for machine vision, Audio signal processing.

UNIT – IV

Networking Basics:

Sockets, ports, UDP, TCP/IP, client server model, socket programming, 802.11, Bluetooth, ZigBee, SSH, firewalls, network security.

UNIT – V

IA32 Instruction Set: application binary interface, exception and interrupt handling, interrupt latency, assemblers, assembler directives, macros, simulation and debugging tools.

TEXT BOOKS

1. Peter Barry and Patrick Crowley, "Modern Embedded Computing", 1st Edition., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine
4. Intel® 64 and IA-32 Architectures Software Developer Manuals

REFERENCE BOOKS

1. Abraham Silberschatz, Peter B. Galvin and Greg Gagne, "Operating System Concepts", Wiley
2. Maurice J. Bach, "The Design of the UNIX Operating System", Prentice-Hall
3. W. Richard Stevens, "UNIX Network Programming", Pearson

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(1855PC05) SYSTEM ON CHIP ARCHITECTURE (PC - 5)

L T P C
4 0 0 4

UNIT – I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II

Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III

Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT –IV

Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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(1855PC06) SENSORS AND ACTUATORS (PC - 6)

L	T	P	C
4	0	0	4

UNIT - I

Sensors / Transducers: Principles, Classification, Parameters, Characteristics, Environmental Parameters (EP), Characterization.

Mechanical and Electromechanical Sensors: Introduction, Resistive Potentiometer, Strain Gauge, Resistance Strain Gauge, Semiconductor Strain Gauges, Inductive Sensors- Sensitivity and Linearity of the Sensor, Types- Capacitive Sensors, Electrostatic Transducer, Force/Stress Sensors using Quartz Resonators, Ultrasonic Sensors.

UNIT - II

Thermal Sensors: Introduction, Gas thermometric Sensors, Thermal Expansion Type Thermometric Sensors, Acoustic Temperature Sensor, Dielectric Constant and Refractive Index Thermo-sensors, Helium Low Temperature Thermometer, Nuclear Thermometer, Magnetic Thermometer, Resistance Change Type Thermometric Sensors, Thermo-EMF Sensors, Junction Semiconductor Types, Thermal Radiation Sensors, Quartz Crystal Thermo-electric Sensors, NQR Thermometry, Spectroscopic Thermometry, Noise Thermometry, Heat Flux Sensors.

Magnetic Sensors: Introduction, Sensors and the Principles Behind, Magneto-resistive Sensors, Anisotropic Magneto-resistive Sensing, Semiconductor Magneto-resistors, Hall Effect and Sensors, Inductance and Eddy Current Sensors, Angular/Rotary Movement Transducers, Synchros, Synchroresolvers, Eddy Current Sensors, Electromagnetic Flowmeter, Switching Magnetic Sensors, SQUID Sensors.

UNIT - III

Radiation Sensors: Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors.

Electro Analytical Sensors: Introduction – The Electrochemical Cell – The Cell Potential – Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media .

UNIT – IV

Smart Sensors: Introduction, Primary Sensors, Excitation, Amplification, Filters, Converters, Compensation, Information Coding/Processing, Data Communication, Standards for Smart Sensor Interface, the Automation.

Sensors Applications: Introduction, On-board Automobile Sensors (Automotive Sensors), Home Appliance Sensors, Aerospace Sensors, Sensors for Manufacturing, Sensors for environmental Monitoring.

UNIT – V

Actuators: Pneumatic and Hydraulic Actuation Systems- Actuation systems, Pneumatic and hydraulic systems, Directional Control valves, Pressure control valves, Cylinders, Servo and proportional control valves, Process control valves, Rotary actuators, Mechanical Actuation Systems- Types of motion, Kinematic chains, Cams, Gears, Ratchet and pawl, Belt and chain drives, Bearings, Mechanical aspects of motor selection, Electrical Actuation Systems, Electrical systems, Mechanical switches, Solid-state switches, Solenoids, D.C. Motors, A.C. Motors, Stepper motors.

TEXT BOOKS:

1. D. Patranabis, "Sensors and Transducers", PHI Learning Private Limited.
2. W. Bolton, "Mechatronics", Pearson Education Limited.

REFERENCE BOOKS:

1. Patranabis, "Sensors and Actuators", 2nd Edition, PHI, 2013.

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(1855PE07) DESIGN FOR TESTABILITY (PE - 3)

L	T	P	C
3	0	0	3

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT – IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-PerScan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, V. D. Agrawal, "Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design", Jaico Publishing House.
2. P. K. Lala, "Digital Circuits Testing and Testability", Academic Press.

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(1855PE08) WIRELESS COMMUNICATIONS AND NETWORKS (PE - 3)

L	T	P	C
3	0	0	3

UNIT – I

The Cellular Concept-System Design Fundamentals: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies- Prioritizing Handoffs, Practical Handoff Considerations, Interference and system capacity – Co channel Interference and system capacity, Channel planning for Wireless Systems, Adjacent Channel interference , Power Control for Reducing interference, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems- Cell Splitting, Sectoring .

UNIT – II

Mobile Radio Propagation: Large-Scale Path Loss: Introduction to Radio Wave Propagation, Free Space Propagation Model, Relating Power to Electric Field, The Three Basic Propagation Mechanisms, Reflection-Reflection from Dielectrics, Brewster Angle, Reflection from prefect conductors, Ground Reflection (Two-Ray) Model, Diffraction-Fresnel Zone Geometry, Knife-edge Diffraction Model, Multiple knife-edge Diffraction, Scattering, Outdoor Propagation Models- LongleyRyce Model, Okumura Model, Hata Model, PCS Extension to Hata Model, Walfisch and Bertoni Model, Wideband PCS Microcell Model, Indoor Propagation Models-Partition losses (Same Floor), Partition losses between Floors, Log-distance path loss model, Ericsson Multiple Breakpoint Model, Attenuation Factor Model, Signal penetration into buildings, Ray Tracing and Site Specific Modeling.

UNIT – III

Mobile Radio Propagation: Small –Scale Fading and Multipath: Small Scale Multipath propagation-Factors influencing small scale fading, Doppler shift, Impulse Response Model of a multipath channel- Relationship between Bandwidth and Received power, Small-Scale Multipath Measurements-Direct RF Pulse System, Spread Spectrum Sliding Correlator Channel Sounding, Frequency Domain Channels Sounding, Parameters of Mobile Multipath Channels-Time Dispersion Parameters, Coherence Bandwidth, Doppler Spread and Coherence Time, Types of Small-Scale Fading-Fading effects Due to Multipath Time Delay Spread, Flat fading, Frequency selective fading, Fading effects Due to Doppler Spread-Fast fading, slow fading, Statistical Models for multipath Fading Channels-Clarke's model for flat fading, spectral shape due to Doppler spread in Clarke's model, Simulation of Clarke and Gans Fading Model, Level crossing and fading statistics, Two-ray Rayleigh Fading Model.

UNIT – IV

Equalization and Diversity: Introduction, Fundamentals of Equalization, Training A Generic Adaptive Equalizer, Equalizers in a communication Receiver, Linear Equalizers, Nonlinear Equalization Decision Feedback Equalization (DFE), Maximum Likelihood Sequence

Estimation (MLSE) Equalizer, Algorithms for adaptive equalization-Zero Forcing Algorithm, Least Mean Square Algorithm, Recursive least squares algorithm. Diversity Techniques-Derivation of selection Diversity improvement, Derivation of Maximal Ratio Combining improvement, Practical Space Diversity Consideration-Selection Diversity, Feedback or Scanning Diversity, Maximal Ratio Combining, Equal Gain Combining, Polarization Diversity, Frequency Diversity, Time Diversity, RAKE Receiver.

UNIT – V

Wireless Networks: Introduction to wireless Networks, Advantages and disadvantages of Wireless Local Area Networks, WLAN Topologies, WLAN Standard IEEE 802.11,IEEE 802.11 Medium Access Control, Comparision of IEEE 802.11 a,b,g and n standards, IEEE 802.16 and its enhancements, Wireless PANs, HiperLan, WLL.

TEXT BOOKS:

1. Theodore, S. Rappaport, "Wireless Communications, Principles, Practice", 2nd Ed., 2002, PHI.
2. Andrea Goldsmith, "Wireless Communications", 2005 Cambridge University Press.
3. KavehPahLaven and P. Krishna Murthy, "Principles of Wireless Networks", 2002, PE
4. GottapuSasibhushana Rao, "Mobile Cellular Communication", Pearson Education, 2012.

REFERENCE BOOKS:

1. KamiloFeher, "Wireless Digital Communications", 1999, PHI.
2. William Stallings, "Wireless Communication and Networking", 2003, PHI.

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(1855PE09) SCRIPTING LANGUAGES (PE - 3)

L	T	P	C
3	0	0	3

UNIT - I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Builtin functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT - II

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT - III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT – IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nutsand-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT – V

TK and JavaScript: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. David Barron, "The World of Scripting Languages", Wiley Student Edition, 2010.
2. Brent Welch, Ken Jones and Jeff Hobbs., "Practical Programming in Tcl and Tk", 4th Edition, Prentice Hall

3. Herbert Schildt, "Java the Complete Reference", 7th Edition, TMH.

REFERENCE BOOKS:

1. ClifFlynt, "Tcl/Tk: A Developer's Guide", 2003, Morgan Kaufmann Series.
2. John Ousterhout, "Tcl and the Tk Toolkit", 2nd Edition, 2009, Kindel Edition.
3. WojciechKocjan and PiotrBeltowski, "Tcl 8.5 Network Programming book", Packt Publishing.
4. Bert Wheeler, "Tcl/Tk 8.5 Programming Cookbook", 2011, Packt Publishing Limited.

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(1855PE10) ADVANCED DIGITAL SIGNAL PROCESSING (PE - 4)

L	T	P	C
3	0	0	3

UNIT – I

Review of DFT, FFT, IIR Filters and FIR Filters: Introduction to filter structures (IIR & FIR).Implementation of Digital Filters, specifically 2nd Order Narrow Band Filter and 1st Order All Pass Filter. Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT – II

Non-Parametric Methods: Estimation of spectra from finite duration observation of signals, Nonparametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods

UNIT - III

Parametric Methods: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Walker & Burg Methods, MA & ARMA models for power spectrum estimation, Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

UNIT – IV

Multi Rate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion. Examples of up-sampling using an All Pass Filter.

UNIT – V

Applications of Multi Rate Signal Processing: Design of Phase Shifters, Interfacing of Digital Systems with Different Sampling Rates, Implementation of Narrow Band Low Pass Filters, Implementation of Digital Filter Banks, Sub-band Coding of Speech Signals, Quadrature Mirror Filters, Transmultiplexers, Over Sampling A/D and D/A Conversion.

TEXT BOOKS:

1. .G. Proakis& D. G. Manolakis, "Digital Signal Processing: Principles, Algorithms & Applications", J 4th Edition, PHI.
2. Alan V Oppenheim & Ronald W Schaffer, "Discrete Time signal processing", PHI.

3. Emmanuel C. Ifeacher, Barrie. W. Jervis, "DSP – A Practical Approach", 2nd Edition, Pearson Education.

REFERENCE BOOKS:

1. S. M .Kay, "Modern spectral Estimation: Theory & Application" 1988, PHI.
2. P. P. Vaidyanathan, "Multi Rate Systems and Filter Banks", Pearson Education.
3. Kaluri V. Rangarao, Ranjan K. Mallik, "Digital Signal Processing: A Practitioner's Approach", ISBN: 978-0-470-01769-2, 210 pages, November 2006 John Wiley.
4. S. Salivahanan, A. Vallavaraj, C. Gnanapriya, "Digital Signal Processing", 2000,TMH

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(1855PE11) NETWORK SECURITY AND CRYPTOGRAPHY (PE - 4)

L	T	P	C
3	0	0	3

UNIT- I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security, Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques.

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Block Cipher Design Principles.

UNIT- II

Encryption Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, Characteristics of Advanced Symmetric block ciphers.

Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

UNIT - III

Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

Number Theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

UNIT - IV

Message Authentication and Hash Functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm. Digital signatures and Authentication protocols: Digital signatures, Authentication Protocols, Digital signature standards.

Authentication Applications: Kerberos, Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT – V

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Key Management. Web Security: Web Security requirements, secure sockets layer and Transport layer security, Secure Electronic Transaction.

Intruders, Viruses and Worms: Intruders, Viruses and Related threats. **Fire Walls:** Fire wall Design Principles, Trusted systems.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security: Principles and Practice", Pearson Education.
2. William Stallings, "Network Security Essentials (Applications and Standards)", Pearson Education.

REFERENCE BOOKS:

1. Eric Maiwald, "Fundamentals of Network Security", Dreamtech press.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security - Private Communication in a Public World", Pearson/PHI.
3. Whitman, "Principles of Information Security", Thomson.
4. Robert Bragg, Mark Rhodes, "Network Security: The complete reference", TMH
5. Buchmann, "Introduction to Cryptography", Springer.

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(1855PE12) HARDWARE SOFTWARE CO-DESIGN (PE - 4)

L	T	P	C
3	0	0	3

UNIT – I

Co - Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co - Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT – II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT – IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT – V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, "Hardware / Software Co- Design Principles and Practice", Wayne Wolf, 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co- Design", 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co-design", 2010, Springer

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(1855PC32) ADVANCED EMBEDDED SYSTEMS LAB

L	T	P	C
0	0	3	2

The following programs to understand the use of RTOS with ARM Processor on IDE Environment Arm Tool chain and Library:

1. Create an application that creates two tasks that wait on a timer whilst the main task loops.
2. Write an application that creates a task which is scheduled when a button is pressed, which illustrates the use of an event set between an ISR and a task.
3. Write an application to demonstrates the Interruptible ISRs(Requires timer to have higher priority than external interrupt button
4. Write an application to test message queues and memory blocks
5. Write an application to test byte queues
6. Write an application that creates two tasks of the same priority and sets the time slice period to illustrate time slicing

Interfacing Programs:

7. Write an application that creates two tasks to blinking two different LEDs at different timings.
8. Write an application that creates two tasks displaying two different messages in LCD displays in two lines
9. Sending messages to mailbox by one task and reading the message from mailbox by another task
10. Sending messages to PC through serial port by three different tasks on priority basis
11. Basic Audio processing on IDE environment
12. Design and Simulation of Adder, Logic Gates, Decoders, Multiplexers, Flip-flops, Counters on FPGA Board.